REMARKS

Claims 7-33 are pending.

The Examiner objected to the drawings because they included a reference sign not mentioned in the description, specifically, "26c" in Fig. 1A. Accordingly, Applicants have amended the specification to change "26d" to --26c--. Accordingly, it is respectfully requested that the objection be withdrawn.

The Examiner suggested a new title that is more descriptive. Accordingly, Applicants have changed the title in accordance with the Examiner's suggestion.

Claims 7, 8, 13-16, 21-24, 29 and 30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams et al. (U.S. Patent No. 6, 307,755).

Claim 9-12, 17-20 and 25-28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Williams et al. as applied to claims 7, 15 and 23, and further in view of Ishibashi (U.S. Patent No. 5,394,751).

These rejections are respectfully traversed and reconsideration is respectfully requested.

It is respectfully submitted that Williams et al. do not disclose all of the features recited in the claims. Additionally, it is respectfully submitted that Ishibashi does not make up for the deficiencies of Williams et al. and, therefore, it is respectfully submitted that these two references, either alone or in combination, can not render the present claims obvious.

For example, Williams et al. discloses using gold (Au) bumps. In contrast thereto, and as is clearly recited in claims 7, 15 and 23, the present invention involves attaching a bumped die that includes a source and gate solder bump array. Furthermore, Williams et al. and Ishibashi do not disclose reflowing the solder as recited in claims 10, 20, 26 and 28.

Additionally, Applicants have added new claims 31-33 which are directed to a further feature of the present invention. The claims are directed to the use of aligners

and corresponding holes for aligning the rails during the manufacturing process. Support for these claims may be found on at least page 6 of the specification and at least in Fig. 7.

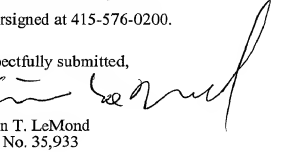
Accordingly, it is respectfully submitted that for the above reasons, neither Williams et al. nor Ishibashi, either alone or in combination, teach, disclose or even suggest a method of making a chip device as recited in the claims. Accordingly, it is respectfully requested that the rejections be withdrawn.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

Please change the title so it reads in its entirety **[IMPROVED METHOD OF MAKING A CHIP DEVICE]** METHOD OF PACKAGING A PLURALITY OF DEVICES UTILIZING A PLURALITY OF LEAD FRAMES COUPLED TOGETHER BY RAILS

IN THE SPECIFICATION:

Paragraph beginning at page 4, line 21:

Die 12 is preferably a one-piece item that is often referred to in the art as "bumped die." As can be seen in Figure 1A, a bumped die includes die 12, "under bump material" that serves as an intermediated layer 26 between the top surface of the die and solder bump 22, and the solder bumps themselves. Preferably, the under bump material is one of TiW, Cu, Au or an equivalent. In the example illustrated in Figure 1A, the under bump material is broken into three layers-Cu plating 26a, sputtered Cu 26b and sputtered Ti**[26d]**26c.